VLSI / SOC Testing

Lecture 21

1. Compression Techniques
   - 100,000 vectors in ATE, storing all 100,000 output responses (plus FF state if full-scan) can require huge storage
   - just store a signature
2. Simplest signature: parity (even or odd) for each PO bit stream
   - Problem: aliasing

   Example 1:

3. One's counting signature: actual number of 1's in each PO stream

   Example 2:

4. Transition counting signature: 2 numbers for PO stream
    - count both $0 \rightarrow 1$ and $1 \rightarrow 0$ transitions
5. Linear Feedback Shift Register (LFSR)

6. MISR: Multiple-Input Signature Registers
   - instead of having an LFSR per PO, combine them
   - slightly greater aliasing probability, due to masking

   Example 3:

7. Built-In-Self-Test
   - Positives:
     - No ATEs
     - place TPG directly on chip
     - Avoid ATPG somewhat
     - Technology and fault-model independent
     - Useful for field test and diagnosis
     - At-speed testing
   - Negatives:
     - Fault Coverage sometimes low
     - Hard to determine exact fault coverage (due to aliasing)
     - Hard to diagnose

   Example 4:

8. On-chip TPG
    - Store vectors in ROM:
    - Exhaustive: use of a counter
    - Pseudo-exhaustive:
    - Pseudo-random:
    - Weighted-pseudo-random:
9. LFSR-based TPG
    - want to generate all $2^n - 1$ patterns

10. Weighted pseudo-random TPG
    - to allow different weights
    - add additional boolean logic to LFSR to create weighting

    Example 5:

11. Output Response Analyzer: similar to compression technique with MISR aliasing effects on FC:

12. BIST Architecture: STUMPS (Self-Testing Using MISR and Parallel SRSG

13. BIST Architecture: BILBO (Built-In Logic Block Observation)
    - convert registers in circuit to BILBO registers
    - test the circuit in a pipelined fashion

14. How about storing multiple signatures?

    - architecture similar to STUMPS
    - extreme compaction - possible to store a signature for every pattern
    - ATPG constraints: must make sure fault is detected on odd number of FFs in a particular group (shift vector)
    - eases diagnosis (increased diagnostic resolution) and allows for built-in self diagnosis

15. Delay-Fault BIST
    - Aim: launch transition at every PI and FF, and sensitize (longest possible) path for each transition to a PO or state
    - launch transitions from TPG: only 1-bit change at a time
    - use same ORA to capture signature
16. Low-Power BIST
    - random vectors generally create more activity than functional vectors
    - Aim: derive BIST vectors that create fewer transitions and still achieve similar fault coverage
      – lower power during scan shift
      – lower power during circuit evaluation/simulation